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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,008	ZHONG DONG	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka et al. (U.S. 6,657,249) in view of Rabkin et al. (U.S. 6,812,515).

As to claim 1, Nishioka et al. discloses a method comprising:

(a) defining a first oxidation stop layer ("silicon nitride film" of layer 106 in figure 34; column 1, lines 35-36) above a first semiconductor layer ("floating gate 107" in figure 34; column 1, lines 35-46; column 10, lines 26-34);

(b) providing a first intrinsic silicon layer (silicon substrate 101 for forming silicon oxide film 106 by thermal oxidation; column 2, lines 33-43) on the first oxidation stop layer ("silicon nitride film" of layer 106 in figure 34; column 1, lines 35-36);

(c) oxidizing at least a sublayer portion of the first intrinsic silicon layer so as to thereby create a corresponding and thermally-grown (thermal oxidation; column 2, lines 33-43), first intrinsic silicon oxide sublayer ("silicon oxide film" in layer 106 of figure 34; column 1, lines 35-46) over the first semiconductor layer "floating gate 107" in figure 34; column 1, lines 35-46); and

(d) disposing a second semiconductor layer ("control gate 113" in figure 34; column 1, lines 35-46) above the first intrinsic silicon oxide sublayer ("silicon oxide film" in layer 106 of figure 34; column 1, lines 35-46) so that the first intrinsic silicon oxide sublayer ("silicon oxide film" in

layer 106 of figure 34; column 1, lines 35-46) provides isolation between the first and second semiconductor layers ("floating gate 107" and "control gate 113" in figure 34; column 1, lines 35-46).

Mishawka et al. does not disclose the first and second semiconductor layers are conductively-doped.

Rabkin et al. disclose the floating gate 206 and control gate 210 are doped-polysilicon (see figure 2; column 4, lines 10-26). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to dope the semiconductor layers of Nishioka et al. by providing two doped-polysilicon layers as taught by Rabkin et al. for the purpose of better conducting between the floating gate and control gate in a memory device (see doped poly layers 206 and 210 in figure 2).

As to claim 10, Nishioka et al. disclose the continuing said oxidizing ("thermal oxidation") of the first intrinsic silicon layer (silicon substrate 101 for forming silicon oxide film 106 by thermal oxidation; column 2, lines 33-43) at least until a corresponding first oxidation front crosses into the first oxidation stop layer ("silicon nitride" film; column 1, lines 35-46) so as to thereby perfect formation of silicon dioxide in the thermally-oxidized, first intrinsic silicon layer (see column 2, lines 34-38; lines 56-63).

As to claim 11, Nishioka et al. discloses the continuing said oxidizing ("thermal oxidation" of the first intrinsic silicon layer (silicon substrate 101 for forming silicon oxide film 106 by thermal oxidation; column 2, lines 33-43) yet further so as to consume silicon atoms within the first oxidation stop layer ("silicon nitride film") and so as to thereby produce

additional silicon oxide ("silicon oxide film") from the consumed silicon atoms (see figure 34; column 2, lines 34-38; lines 56-63).

As to claim 12, Nishioka et al. discloses the providing silicon nitride layer ("silicon nitride film") between the first and second conductively-doped semiconductor layers ("floating gate 107" and "control gate 113" in figure 34; column 1, lines 35-46) so that the combination of the silicon nitride layer ("silicon nitride film") and the perfected silicon dioxide in the thermally-oxidized, first intrinsic silicon layer ("silicon substrate 101" for forming silicon oxide film 106 by thermal oxidation; column 2, lines 33-43) provide isolation (three-layer insulator) between the first and second conductively-doped semiconductor layers ("floating gate 107" and "control gate 113" in figure 34; column 1, lines 35-46).

As to claim 13, Nishioka et al. discloses the providing a second silicon oxide layer ("second silicon oxide"; column 1, lines 35-46) between the silicon nitride layer ("silicon nitride film") and the second conductively-doped semiconductor layer ("control gate 113") so that the combination of the second silicon oxide layer ("second silicon film"), the silicon nitride layer ("silicon nitride film") and the perfected silicon dioxide ("silicon oxide film") in the thermally-oxidized ("thermal oxidation"), first intrinsic silicon layer ("silicon substrate 101" for forming silicon oxide film 106 by thermal oxidation; column 2, lines 33-43) provide isolation ("three-layer isolator") between the first and second conductively-doped semiconductor layers ("floating gate 107" and "control gate 113" in figure 34; column 1, lines 35-46).

As to claim 14, Nishioka et al. further disclose: providing a silicon nitride layer ("silicon nitride film", column 1, lines 35-46) between the first and second conductively-doped semiconductor layers ("floating gate 107" and "control gate 113" in figure 34; column 1, lines

35-46) so that the combination of the silicon nitride layer ("silicon nitride film", column 1, lines 35-46) and the first intrinsic silicon oxide sublayer (silicon substrate 101 for forming silicon oxide film 106 by thermal oxidation; column 2, lines 33-43) provide isolation (three-layer insulator film) between the first and second conductively-doped semiconductor layers ("floating gate 107" and "control gate 113" in figure 34; column 1, lines 35-46).

As to claim 15, Nishioka et al. further disclose: a second silicon oxide layer ("a second silicon oxide film"; column 1, lines 35-46) between the silicon nitride layer ("silicon nitride film"; column 1, lines 35-46) and the second conductively-doped semiconductor layer ("control gate 113" in figure 34; column 1, lines 35-46) so that the combination of the second silicon oxide layer, the silicon nitride layer ("silicon nitride film"; column 1, lines 35-46) and the first intrinsic silicon oxide sublayer provide isolation (three-layer isolation) between the first and second conductively-doped semiconductor layers ("floating gate 107" and "control gate 113" in figure 34; column 1, lines 35-46).

As to claim 22, Nishioka et al. discloses a method comprising:

(a) defining a first oxidation stop layer ("silicon nitride film" of layer 106 in figure 34; column 1, lines 35-36) above a first semiconductor layer ("floating gate 107" in figure 34; column 1, lines 35-46; column 10, lines 26-34);

(b) providing a an essentially undoped semiconductor layer (silicon substrate 101 for forming silicon oxide film 106 by thermal oxidation; column 2, lines 33-43) on the first oxidation stop layer ("silicon nitride film" of layer 106 in figure 34; column 1, lines 35-36);

(c) oxidizing at least a sublayer portion of the essentially undoped semiconductor layer (106)

so as to thereby create a corresponding, essentially undoped and thermally-grown (thermal oxidation; column 2, lines 33-43), first oxide sublayer ("silicon oxide film" in layer 106 of figure 34; column 1, lines 35-46) over the first semiconductor layer ("floating gate 107" in figure 34; column 1, lines 35-46); and

(d) disposing a second semiconductor layer ("control gate 113" in figure 34; column 1, lines 35-46) above the first oxide sublayer ("silicon oxide film" in layer 106 of figure 34; column 1, lines 35-46) so that the first oxide sublayer ("silicon oxide film" in layer 106 of figure 34; column 1, lines 35-46) provides electrical isolation between the first and second semiconductor layers ("floating gate 107" and "control gate 113" in figure 34; column 1, lines 35-46).

Mishawka et al. does not disclose the first and second semiconductor layer are conductively-doped.

Rabkin et al. disclose the floating gate 206 and control gate 210 are doped-polysilicon (see figure 2; column 4, lines 10-26). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to dope the semiconductor layers of Nishioka et al. by providing two doped-polysilicon layers as taught by Rabkin et al. for the purpose of better conducting between the floating gate and control gate in a memory device (see doped poly layers 206 and 210 in figure 2).

3. Claim 2, and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka et al. (U.S. 6,657,249) and Rabkin et al. (U.S. 6,812,515) in view of Kobayashi (US 6,346,448).

As to claim 2, Nishioka et al. and Rabkin et al. do not disclose the thermally-grown, first

intrinsic silicon oxide sublayer includes stoichiometric silicon dioxide (SiO.sub.2). Kobayashi discloses an interlayer insulating film comprising silicon dioxide or undoped silicon dioxide (see figure 4; column 5, lines 65-67; column 6, lines 1-5). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide silicon dioxide for the insulating film/layer of Nishioka et al. and Rabkin et al. as taught by Kobayashi et al. for the purpose of reducing inter-gate spacing (see column 1, lines 18-21).

4. Claim 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka et al. (U.S. 6,657,249) and Rabkin et al. (U.S. 6,812,515) and further in view of Lee et al. (US 2005/0074982).

As to claim 3, Nishioka et al. and Rabkin et al. do not disclose a providing step of the first intrinsic silicon layer includes using atomic layer deposition (ALD) to define a thickness of the first intrinsic silicon layer. Lee et al. disclose a providing step of the first intrinsic silicon layer includes using atomic layer deposition (ALD) to define a thickness of the first intrinsic silicon layer (see paragraph 46). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide atomic layer deposition (ALD) to define a thickness of controlled Si composition in Nishioka et al. and Rabkin et al. as taught by Lee et al. for the purpose of controlling the thickness of Si composition (see paragraph 46).

As to claim 4, Nishioka et al. and Rabkin et al. do not disclose said thickness of the first intrinsic silicon layer is in a range of about 15 Angstroms to about 50 Angstroms. Lee et al. disclose said thickness of the first intrinsic silicon layer is in a range of about 15 Angstroms to about 50 Angstroms (wherein the controlled thickness are in the range of approximately 2-60

angstroms (see claim 6). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to a range of thickness of controlled Si composition in Nishioka et al. and Rabkin et al. as taught by Lee et al. for the purpose of controlling a precise thickness of Si composition (see claim 6).

5. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), and Lee et al. (US 2005/0074982) and further in view of Yamazaki et al. (US 2005/0040401).

As to claim 5, Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), and Lee et al. (US 2005/0074982) do not disclose said defining of the first oxidation stop layer includes creating a first silicon nitride composition having a nitrogen concentration of at least about 5% atomic.

Yamazaki et al. disclose said defining of the first oxidation stop layer includes creating a first silicon nitride composition ("silicon nitride oxide film 602a"; figures 6A-8C; paragraph 125) having a nitrogen concentration of at least about 5% atomic (adjusted to at least 25 atomic % to less than 50 atomic %; paragraph 125). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide a percentage range of nitrogen concentration in silicon nitride composition in Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), and Lee et al. (US 2005/0074982) as taught by Yamazaki et al. for the purpose of obtaining an optimized operation during a heat-treatment of the semiconductor device.

As to claim 6, Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), and Lee et

al. (US 2005/0074982) do not disclose said first silicon nitride composition has a nitrogen concentration of at least about 10% atomic.

Yamazaki et al. disclose said first silicon nitride composition has a nitrogen concentration of at least about 10% atomic ("silicon nitride oxide film 602a"; figures 6A-8C; paragraph 125) having a nitrogen concentration of at least about 5% atomic (adjusted to at least 25 atomic % to less than 50 atomic %; paragraph 125). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide a percentage range of nitrogen concentration in silicon nitride composition in Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), and Lee et al. (US 2005/0074982) as taught by Yamazaki et al. for the purpose of obtaining an optimized operation during a heat-treatment of the semiconductor device.

6. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), Lee et al. (US 2005/0074982), Yamazaki et al. (US 2005/0040401) and further in view of Yu et al. (US 6566205).

As to claim 7, Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), Lee et al. (US 2005/0074982), and Yamazaki et al. (US 2005/0040401) do not disclose said creating of the first silicon nitride composition includes using Decoupled Plasma Nitridation (DPN) to introduce nitrogen into the first conductively-doped semiconductor layer.

Yu et al. disclose said creating of the first silicon nitride composition includes using Decoupled Plasma Nitridation (DPN) to introduce nitrogen into the first conductively-doped semiconductor layer (see column 2, lines 13-16; column 3, lines 28-35). Therefore, it would have

been obvious to a person having ordinary skill in the art at the time the invention was made to provide Decoupled Plasma Nitridation (DPN) to introduce nitrogen into a conductively-doped semiconductor layer in Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), Lee et al. (US 2005/0074982), and Yamazaki et al. (US 2005/0040401) as taught by Yu et al. for the purpose of obtaining a FET gate capable of operating at low voltages and having a minimum of trapped charge in a dielectric portion (see column 2, lines 13-16; column 3, lines 28-35).

As to claim 8, Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), Lee et al. (US 2005/0074982), and Yamazaki et al. (US 2005/0040401) do not disclose said creating of the first silicon nitride composition includes using Remote Plasma Nitridation (RPN) to introduce nitrogen into the first conductively-doped semiconductor layer.

Yu et al. disclose said creating of the first silicon nitride composition includes using Remote Plasma Nitridation (RPN) to introduce nitrogen into the first conductively-doped semiconductor layer (see column 2, lines 13-16; column 3, lines 21-27). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to provide Remote Plasma Nitridation (RPN) for introducing nitrogen into a conductively-doped semiconductor layer in Nishioka et al. (U.S. 6,657,249), Rabkin et al. (U.S. 6,812,515), Lee et al. (US 2005/0074982), and Yamazaki et al. (US 2005/0040401) as taught by Yu et al. for the purpose of obtaining a FET gate capable of operating at low voltages and having a minimum of trapped charge in a dielectric portion.

As to claim 9, Kobayashi et al. disclose said creating of the first silicon nitride composition includes using ion implant "(ion implantation"; column 8, lines 42-50) to introduce nitrogen into the first conductively-doped semiconductor layer (see column 8, lines 42-50).

Response to Arguments

7. Applicant's arguments with respect to claim 22 has been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that layer 106 of Nishioka et al is not an intrinsic silicon layer (essentially undoped silicon layer).

In response, the examiner does not agree with applicant's argument because Nishioka et al clearly discloses in figure 34, column 2, lines 33-43, the layer 106 is only a "silicon oxide film" and it is not a doped layer, thus layer 106 is considered as an essentially undoped silicon layer because layer 106 only includes "silicon oxide" material and not include any other doped material (see figure 34, column 2, lines 33-43).

Applicant further argued: "it is clear that errors have been made with respect to the teachings of Nishioka and the motivation to combine with Rabkin".

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Nishioka clearly discloses all the limitations (e.g., claims 1 and 22 as set forth

above), except for the first and second semiconductor layers are conductively-doped. However, Rabkin et al. disclose the floating gate 206 and control gate 210 are doped-polysilicon (see figure 2; column 4, lines 10-26). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to dope the semiconductor layers of Nishioka et al. by providing two doped-polysilicon layers as taught by Rabkin et al. for the purpose of better conducting between the floating gate and control gate in a memory device (see doped poly layers 206 and 210 in figure 2).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
May 21, 2004